REMARKS

Declaration

The addresses given for the inventors are complete in that any mail addressed to those addresses can reach the inventors. Thus, it is submitted that no correction is required and that declaration is not defective.

Claim Amendments

Claims 18 to 23 have been examined. Claims 1 to 17 and 24 to 27 have been withdrawn from consideration and are canceled. Claim 18 is also canceled. Claims 19 and 21 have been amended to correct informalities and to conform to US claiming style. Also, claims 19 and 21 have been amended to include the feature of claim 18. Furthermore, claim 22 has been rewritten in independent form.

New dependent claims 28 to 33 have been added. Claims 28 and 29 are supported, for example, by Fig. 13 and its corresponding description in the specification. Claims 30 to 33 are supported by original claim 21. No new matter has been added.

Therefore, claims 19 to 33 are pending. No new matter has been added.

Claim Rejections – 35 USC §102

Claims 18 to 21 have been rejected as being anticipated by Noto et al. Claim 18 has been deleted. Applicants submit the claims 19 to 21 are not anticipated by the cited prior art for the following reasons. First, claim 19 is addressed. Claim 19 has been amended to recite as follows:

> 19. (Currently Amended) A semiconductor device comprising:
> an upper layer wiring;
> a pad portion disposed above the upper layer wiring;
> an interlayer insulating film disposed below the upper layer wiring;
> a lower layer wiring disposed below the interlayer insulating film; and

a hole in the interlayer insulating film, connecting the upper layer wiring and the lower layer wiring, said hole being formed not under but laterally spaced away from the pad portion,

wherein no hole connecting the upper layer wiring and the lower layer wiring is formed under the pad portion. (Emphasis added.)

The bolded feature is not disclosed, taught, or suggested by the cited prior art. The present invention as claimed in claim 19 is a device that has a hole in the interlayer insulating film, connecting the upper layer wiring and the lower layer wiring. The hole is formed not under the pad portion but laterally spaced away from the pad portion; AND no hole connects the upper layer wiring to the lower layer wiring under the pad portion. Noto et al., in contrast, discloses in Fig. 22 a sectional view of a region where the bonding pad and I/O cell of the semiconductor chip is encapsulated in the TCP (Tape Carrier Package), in which a semiconductor chip is formed with a microcomputer. What is absent in Fig.. 22 is a hole in the interlayer insulating film, connecting the upper layer wiring and the lower layer wiring, the hole being formed not under but laterally spaced away from the pad portion, as recited in claim 19. Noto's Fig. 4, on the other hand, shows a through hole 14 and through hole 16 disposed under the bonding pad BP, which is what the present invention disclaims. These and other remaining figures do not disclose the presently claimed invention. Thus, the present invention as claimed in claim 19 is not anticipated by Noto et al. for the foregoing reasons.

It should also be emphasized that there is no teaching or suggestion to incorporate the structure of Fig. 22 into the structure in Fig. 4 and vice versa. Fig. 22 discloses a sectional view of a region where the bonding pad and I/O cell of the semiconductor chip is encapsulated in the TCP (Tape Carrier Package). In contrast Fig. 4 discloses a sectional view of the signal input cell and the corresponding bonding pad of the CMOS gate array. There is no teaching, motivation, or suggestion to combine these disparate structures.

Claims 20, 29 and 30 depending from claim 19 are not anticipated at least for the same reasons as claim 19.

Claim 21 as amended recites:

21. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate;
a gate oxide film provided over the semiconductor substrate;
a gate electrode formed on the gate oxide film;
a source/drain region formed in the semiconductor substrate and disposed adjacent to the gate electrode;
a lower layer wiring connected to the source/drain region with contact;
an interlayer insulating film covering the lower layer wiring;
a hole formed in an interlayer insulating film; and
an upper layer wiring having a pad portion, disposed over the interlayer insulating film and connected to the lower layer wiring through the hole,
wherein no hole connecting the upper layer wiring and the lower layer wiring is formed under the pad portion.

Noto et al. does not disclose the bolded features above as explained for claim 19. Therefore, claim 21 is also not anticipated.

Claims 23, 28, and 31 to 33 depend directly or indirectly from claim 21. Therefore, at least for the same reasons claim 21, these claims are not anticipated.

Allowable Claims

Claims 22 and 23 have been deemed to be allowable if rewritten in independent form. Claim 22 has been rewritten in independent form including all of limitations of base claim 21. Thus, claim 22 is believed to be allowable.

Therefore, for the foregoing reasons, all of the pending claims are believed to be allowable.